



450100-02936

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Taku YAMAGATA et al.
Serial No. : 09/771,743
For : TIMING ERROR DETECTION CIRCUIT, DEMODULATION
CIRCUIT AND METHODS THEREOF
Filed : January 29, 2001
Notice of Allowance : August 1, 2005
Examiner : Sudhanshu C. Pathak
Art Unit : 2634
Conf. No. : 1150

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Box 1450, Alexandria, VA 22313-1450, on September 7, 2005.

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Name of Applicant, Assignee or Registered Representative

Thomas F. Presson
Signature

September 7, 2005

Date of Signature

RESPONSE TO EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

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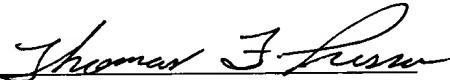
Sir:

This is in response to the Examiner's Statement of Reasons for Allowance, which
accompanied the Notice of Allowance mailed August 1, 2005. To the extent the Examiner's

Statement of Reasons for Allowance states, implies or is construed to mean that the claims are allowable over the prior art of record because the Examiner believes the claims should be interpreted to include one or more features or limitations not recited therein, Applicants' attorney disagrees with such an interpretation. Moreover, it is Applicants' contention that there is no particular limitation in the allowed claims that is more critical than any other. The issuance of the Examiner's Statement of Reasons for Allowance should not be construed as a surrender by Applicants of any subject matter. It is the intent of Applicants, by their attorney, to construe the allowed claims so as to cover the invention disclosed in the instant application and all equivalents to which the claimed invention is entitled.

Respectfully submitted,

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By 
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